WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a control block comprising:

a first series of delay elements coupled to a reference clock input;

a phase detector coupled to the reference clock input and an output of the first series of delay elements; and

a counter coupled to the phase detector and the series of delay elements;

a storage circuit coupled to the control block and the output of the first series of delay elements; and

a delay circuit coupled to the storage circuit.

2. The integrated circuit of claim 1 wherein the storage circuit comprises a plurality of flip-flops having an input coupled to the counter in the control block, an output coupled to the delay circuit, and a clock input coupled to an output of the delay circuit.

3. The integrated circuit of claim 1 wherein the storage circuit comprises:

a logic gate coupled to an input and the output of the delay circuit, and further coupled to a latch, the latch coupled between the counter in the control circuit and the delay circuit.

4. The integrated circuit of claim 1 wherein the delay circuit comprises a series of delay elements, each having an input and an output,

wherein the storage circuit comprises a logic gate coupled to an input of a delay element in the delay circuit and an output of a delay element in the delay circuit, and further coupled to a latch, the latch coupled between the counter in the control circuit and the delay circuit.

5. The integrated circuit of claim 4 wherein the logic gate is an exclusive-OR gate.

6. The integrated circuit of claim 1 wherein the delay circuit is a delay element.

7. The integrated circuit of claim 6 further comprising:

a first register having a clock input coupled to an output of the delay circuit; and

a second register having a complementary clock input coupled the output of the delay circuit.

8. The integrated circuit of claim 7 wherein the first register has a first input and the second register has a second input, and the first and second inputs are coupled to a data input.

9. The integrated circuit of claim 8 wherein the integrated circuit is a field programmable gate array.

10. An integrated circuit comprising:

a control circuit configured to receive a reference clock and provide a plurality of control bits;

a storage circuit coupled to receive and store the plurality of control bits, and further configured to provide the plurality of stored control bits; and

a delay element configured to receive the plurality of stored control bits.

11. The integrated circuit of claim 10 wherein the control circuit comprises:

a first series of delay elements configured to receive the reference clock;

a phase detector configured to compare the phases of the reference clock and an output of the first series of delay elements and provide an output signal; and

a counter configured to receive the phase detector output and provide the control bits.

12. The integrated circuit of claim 11 wherein a polarity of the phase detector output depends on the relative phase of the reference clock and the output of the first series of delay elements, and the counter is an up-down counter that counts up when the phase detector output has a first polarity, and counts down when the phase detector output has a second polarity.

13. The integrated circuit of claim 10 wherein the storage circuit comprises a plurality of flip-flops, each flip-flop having an input configured to receive and store one of the

plurality of control bits, and further configured to provide the stored one of the plurality of control bits to the delay element.

14. The integrated circuit of claim 13 wherein each of the plurality of flip-flops in the storage circuit has a clock input configured to receive the output of the delay element.

15. The integrated circuit of claim 11 further comprising a second series of delay elements including the delay element, each delay element in the second series of delay elements having an input, and

wherein the storage circuit comprises a logic gate configured to receive a signal from an input of a delay element in the second series of delay elements and an output of the second series of delay elements, and further configured to provide an output to a plurality of latches, each latch configured to receive and store one of the plurality of control bits, and further configured to provide the stored one of the plurality of control bits to the delay element.

16. The integrated circuit of claim 15 wherein the logic gate comprises an exclusive-OR gate.

17. The integrated circuit of claim 10 wherein the control circuit is a delay-locked loop.

18. A method of delaying a data strobe signal comprising:

receiving a reference clock signal;

delaying the reference clock signal a first duration, the first duration dependent on a plurality of control signals;

comparing the phase the reference clock signal and the delayed reference clock signal to generate the plurality of control signals;

storing the plurality of control signals;

receiving a data strobe signal; and

delaying the data strobe signal a second duration, the second duration dependent on the plurality of stored control signals.

19. The method of claim 18 wherein the plurality of control signals are stored when the received data strobe signal has been delayed the second duration.

20. The method of claim 18 wherein the plurality of control signals are stored when an edge of the data strobe signal is not being delayed.